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Performance of Different Full Adder Structures for Optimized Design

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ABSTRACT

Design of high performance and energy efficient digital systems are one of the most important research areas in VLSI system design which is suitable for real-time applications. One of the functional elements used in complex arithmetic circuits is an adder. To design an energy efficient adder one-bit full adder cell is designed based on adiabatic logic. The proposed ALFA cell is designed using adiabatic logic which results with the negligible amount of exchange of energy with the surrounding environment. Therefore, the application circuits based on this logic will have negligible energy loss due to heat dissipation. It requires 24 transistors to get the true and complimentary arithmetic sum and carry output. The proposed adiabatic logic based full adder (ALFA) cell processes the three single bit inputs and provides the output as sum, carry, sum bar and carry bar in a single architecture. The proposed ALFA cell reduces the power consumption by 98.49%, 90.93%, and 89.37%, respectively, when compared to CMOS full adder, 14T pass-transistor logic (PTL) with transmission gate (TG) full adder and 16T PTL with TG full adder.

Keywords: *Pass transistor logic; Transmission gate; Adiabatic logic; CMOS logic.*

1.0 Introduction

VLSI technology facilitates the designers for embedding more than hundred thousand of gates in a single IC. Achieving power reduction in full adder circuits is essential in handheld and portableVLSI based application circuits. Most of these application circuits incorporate processor-based blocks. Most probably, the circuits inside these blocks have full adder as their main element. Hence, in order to obtain the overall power optimization in a VLSI IC, as an initial attempt, the power reduction in full adders is the prime aim of the VLSI designers. Thus, in order to have an efficient approach, that is to implement the application circuits inside the VLSI. IC provide many choices for describing, synthesizing and verifying the designs with reduced complexity.Depletion of the silicon area during fabrication leads to the decline in power consumption. Thus, choosing low power consuming logic styles in the logical design stage and improving the efficiency of the physical design stage by adopting enhanced placement and routing techniques will yield a low power design with reduced propagation delay.

With this perception, the design and implementation of a low power full adder cell were carried out by selecting the low power consuming logic styles such as CMOS based 28T full adder cell, PTL based 16T full adder cell with TG, PTL based 14T full adder cell with TG and proposed ALFA cell. In VLSI, there is a trade-off between area, power and delay. To overcome these issues, it is necessary to design an optimized design. Hence the ALFA cell is proposed that overcomes the problems of the existing techniques such as CMOS Full Adder, PTL logic and transmission gate. The flow of this paper described full adder using various logic styles, elaborates the less area occupying and low power consuming efficient ALFA cell design approaches, the simulation outputs of the designed full adder cells with the considered logic styles are illustrated along with their respective area and power consumption results.

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN.

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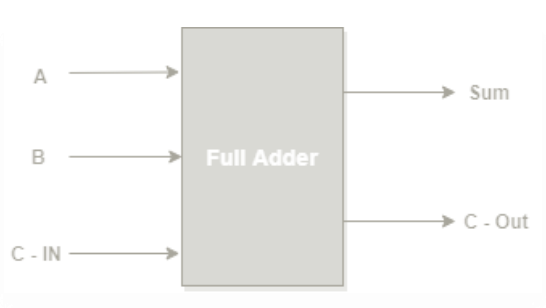
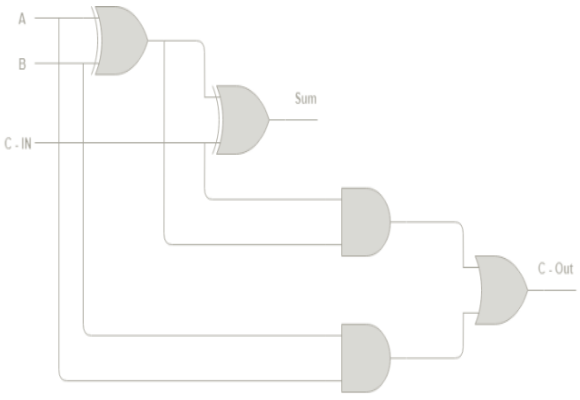
The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

Figure 1: Full Adder Truth Table



Logical Expression for SUM:
= A' B' C-IN + A' B C-IN' + A B' C-IN' + A B C-IN
= C-IN (A' B' + A B) + C-IN' (A' B + A B')
= C-IN XOR (A XOR B)= (1,2,4,7)
Logical Expression for C-OUT:
= A' B C-IN + A B' C-IN + A B C-IN' + A B C-IN
= A B + B C-IN + A C-IN= (3,5,6,7)
Another form in which C-OUT can be implemented:
= A B + A C-IN + B C-IN (A + A')
= A B C-IN + A B + A C-IN + A' B C-IN
= A B (1 +C-IN) + A C-IN + A' B C-IN
= A B + A C-IN + A' B C-IN
= A B + A C-IN (B + B') + A' B C-IN
= A B C-IN + A B + A B' C-IN + A' B C-IN
= A B (C-IN + 1) + A B' C-IN + A' B C-IN
= A B + A B' C-IN + A' B C-IN
= AB + C-IN (A' B + A B')
Therefore COUT = AB + C-IN (A EX – ORB)

Figure 2: Full Adder Logic Circuit

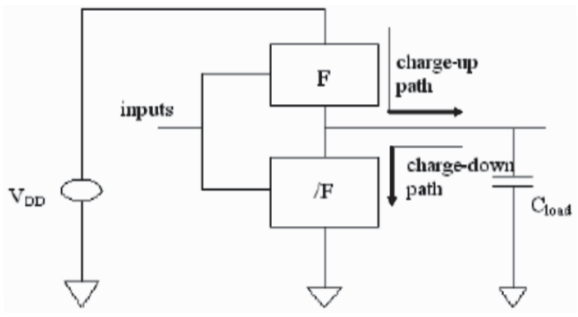


Transmission gates are the fully restoring logic version of PTL whose output logic level does not degrade when passed throughthe respective logic level signal available on its inputs. Hence, in designing the full adder cells with PTL, in order to get the non- degraded outputs of the sum and carry, transmission gates are suitably inserted into thedesigns.

PTL with TG based 16 transistors full adder cell is shown inFig. 2.The simulation results show that the PTL with TG based16T full adder cell has lower power consumption than that of the CMOS based 28T full addercell. The PTL with TG based 14 transistors full adder cell is shown in Fig. 3.It has lower dynamic power consumption when compared

In this we will examine simple circuit configurations which can be used for adiabatic switching. A general circuit topology for the conventional CMOS gates and adiabatic counter parts is shown in Figure 3. To convert a conventional CMOS logic gate into an adiabatic gate, the pull-up transistor and the pull-down transistor networks must be replaced with complementary transmission-gate (T-gate). The T-gate network implementing the pull-up function is used to drive the true output of the adiabatic gate, while the T-gate network implementing the pulldown function drives the complementary output node.

Figure 3: A Simple Adiabatic Logic Gate



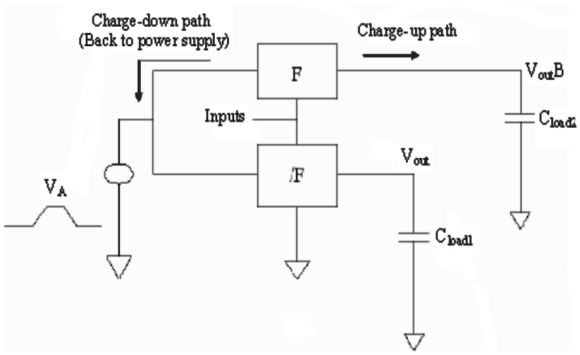


Figure 4: 6T Full Adder

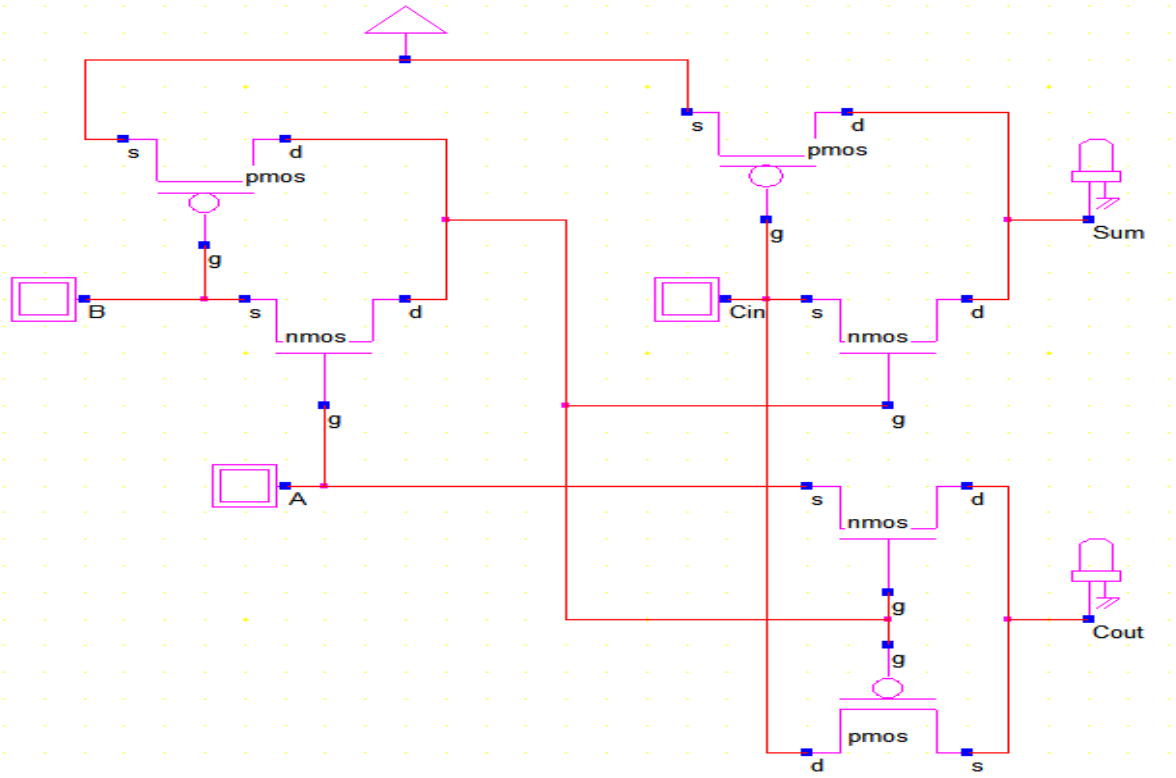
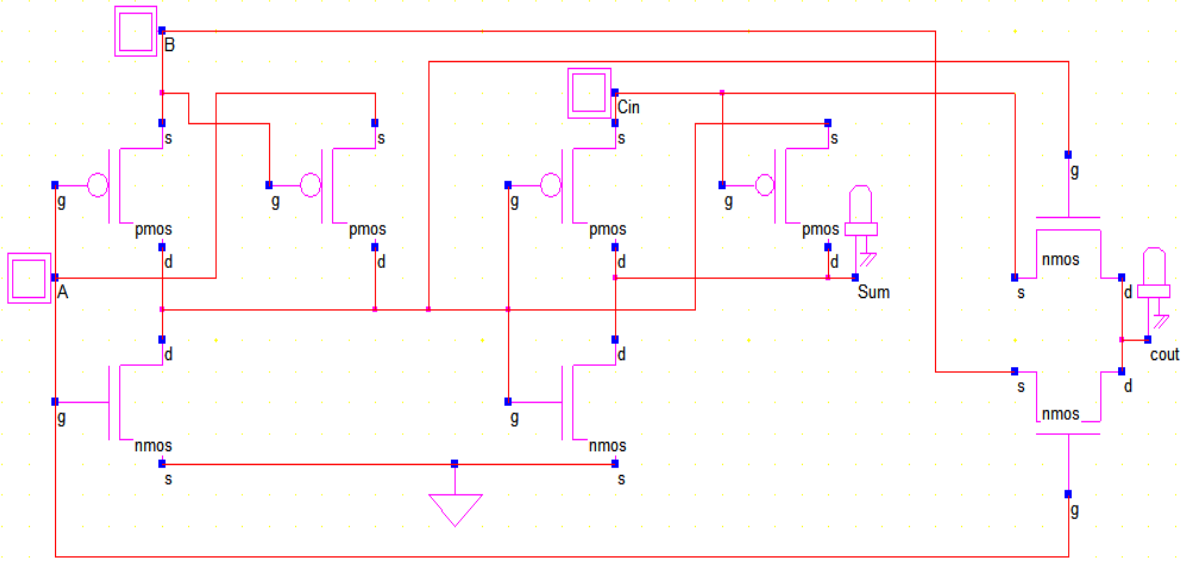
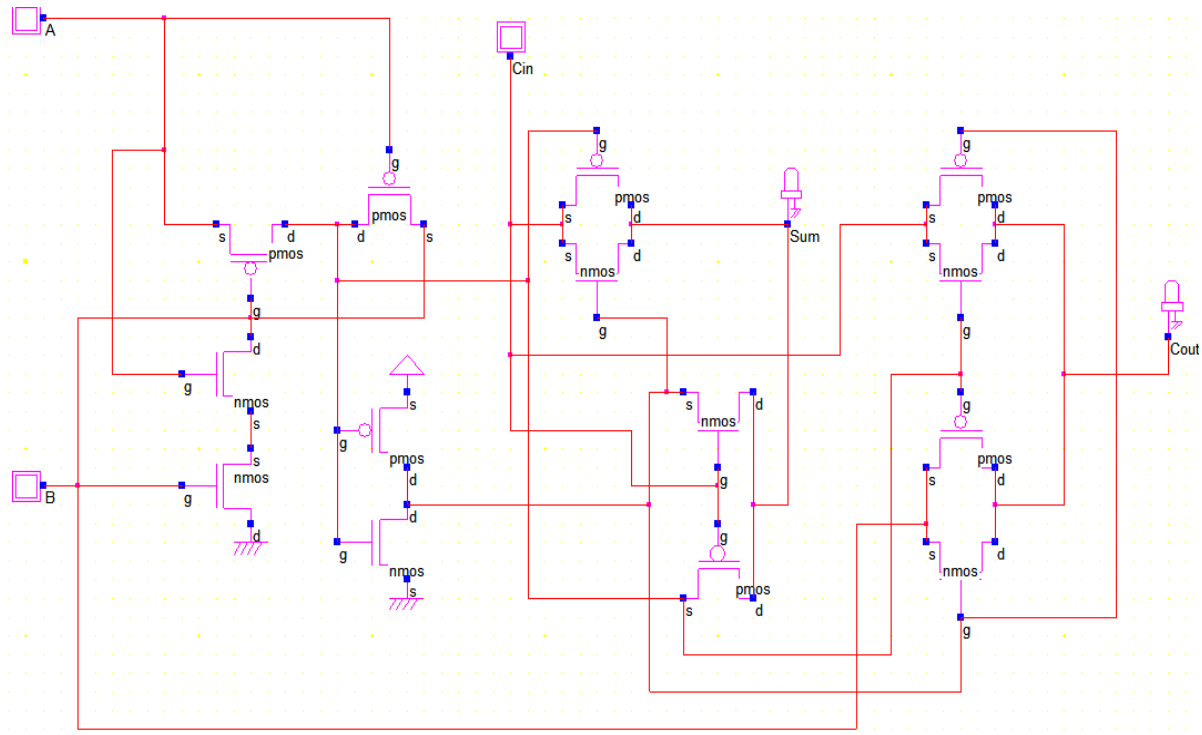


Figure 5: 8T Full Adder



Note that all the inputs should also be available in complementary form. Both the pull-up and pull-down networks in the adiabatic logic circuit are used for charging as well as discharging the output node capacitance, which ensures that the energy stored at the output node can be retrieved by the power supply, at the end of each cycle shown in Figure 4. To allow adiabatic operation, the DC voltage source of the original circuit must be replaced by a varying power supply with the ramped voltage output.

Figure 6: 14T Full Adder



The necessary circuit modifications which are used to convert a conventional CMOS logic circuit into an adiabatic logic circuit increase the device count by a factor of two or even more.

2.0 Adiabatic Logic Families

Adiabatic logic circuits classified into two types: (a) Quasi/ Partial Adiabatic Logic Circuits (b) Full Adiabatic Logic Circuits

a) **Quasi/Partial Adiabatic Logic Circuits:** Quasi- adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of thepower-clock. Popular Partially Adiabatic families include the following:
   a. Efficient Charge Recovery Logic(ECRL).
   b. 2N-2N2P AdiabaticLogic.
   c. Positive Feedback Adiabatic Logic(PFAL).
   d. NMOS Energy Recovery Logic (NERL).
   e. Clocked Adiabatic Logic(CAL).
   f. True Single-Phase Adiabatic Logic (TSEL).
   g. Source-coupled Adiabatic Logic (SCAL).

b) **Full Adiabatic Logic Circuits:** Full-adiabatic circuits have no non-adiabatic loss, but they are much more complex than quasi-adiabatic circuits. All the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed andtheinputspowerclocksynchronization.
Some Fully adiabatic logic families include:
   h. Pass Transistor Adiabatic Logic(PAL).
   i. Split-RailChargeRecoveryLogic(SCRL).

3.0 NMOS Energy Recovery Logic (NERL)

NMOS energy recovery logic (NERL), which uses NMOS transistors only and a simpler6-phase clocked power. Its area over head and energy consumption are smaller, compared with the other fully adiabatic logics. We employed bootstrapped NMOS switches to simplify the NERL circuits. With the simulation results for a full adder, we confirmed that the NERL circuit consumed substantially less energy than the other adiabatic logic circuits at low-speed operation. NERL is more suitable than the other adiabatic logic circuits for the applications that do not require high performance but low energyconsumption. NMOS energy recovery logic gate.

Figure 7: 16T Full Adder

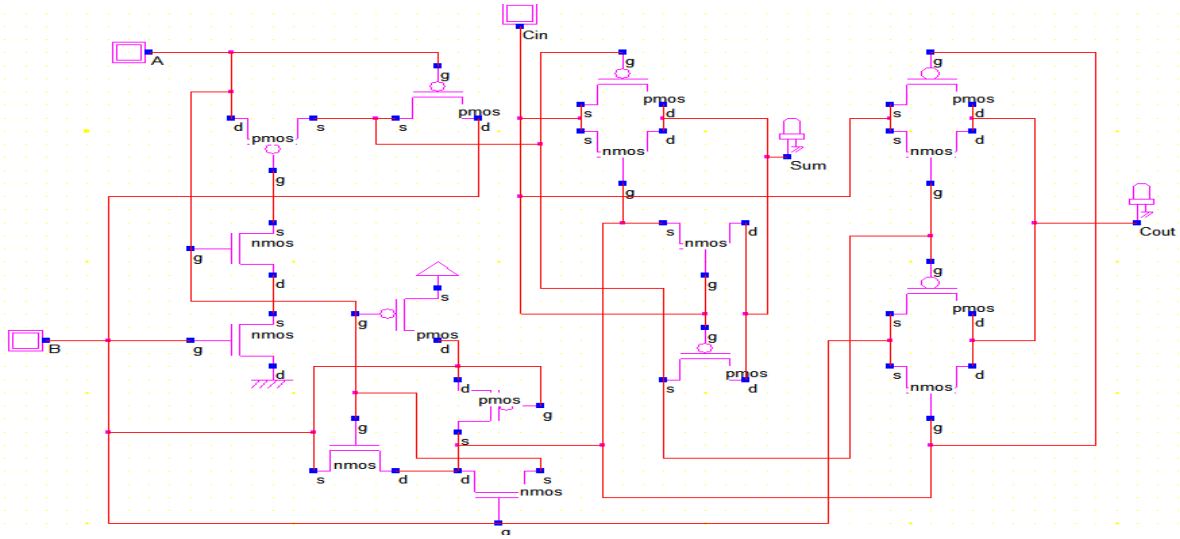


Figure 8: 18T Full Adder

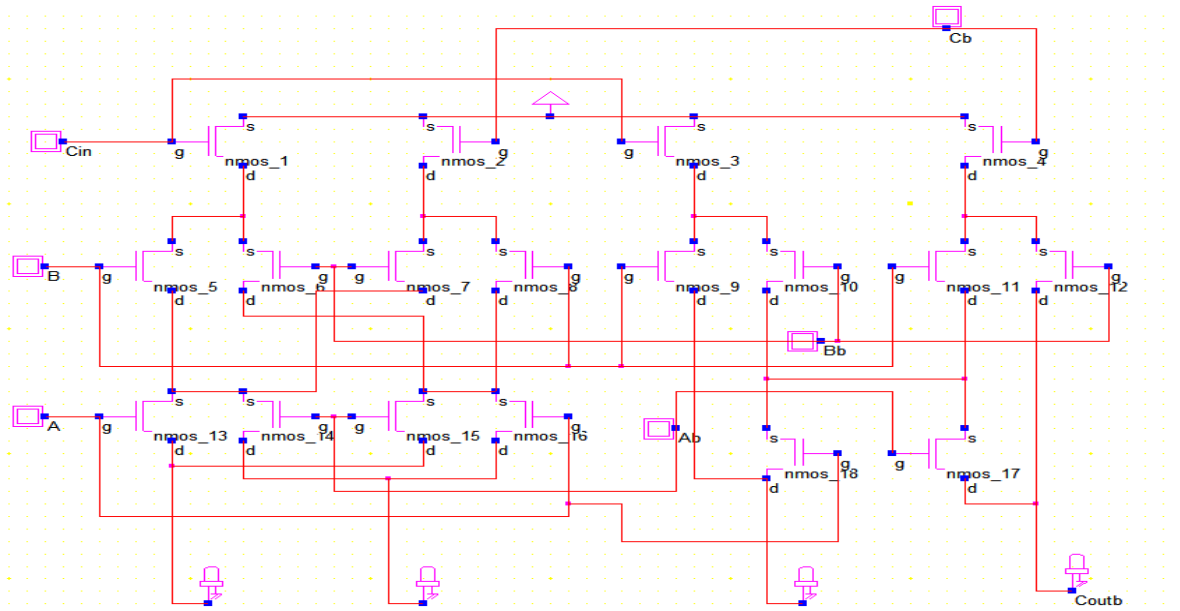


Figure 9: Simulation of 18T ALFA Cell

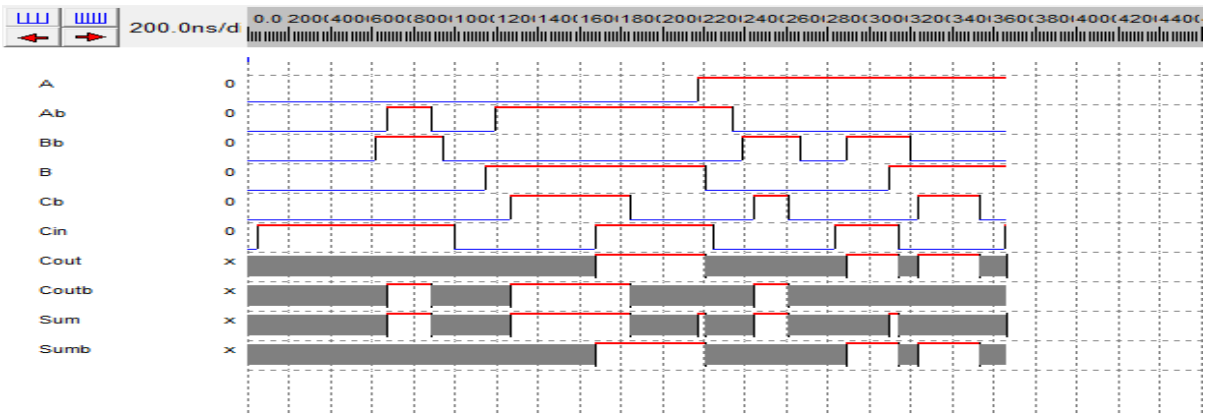


Figure 10: Layout for Proposed ALFA Cell

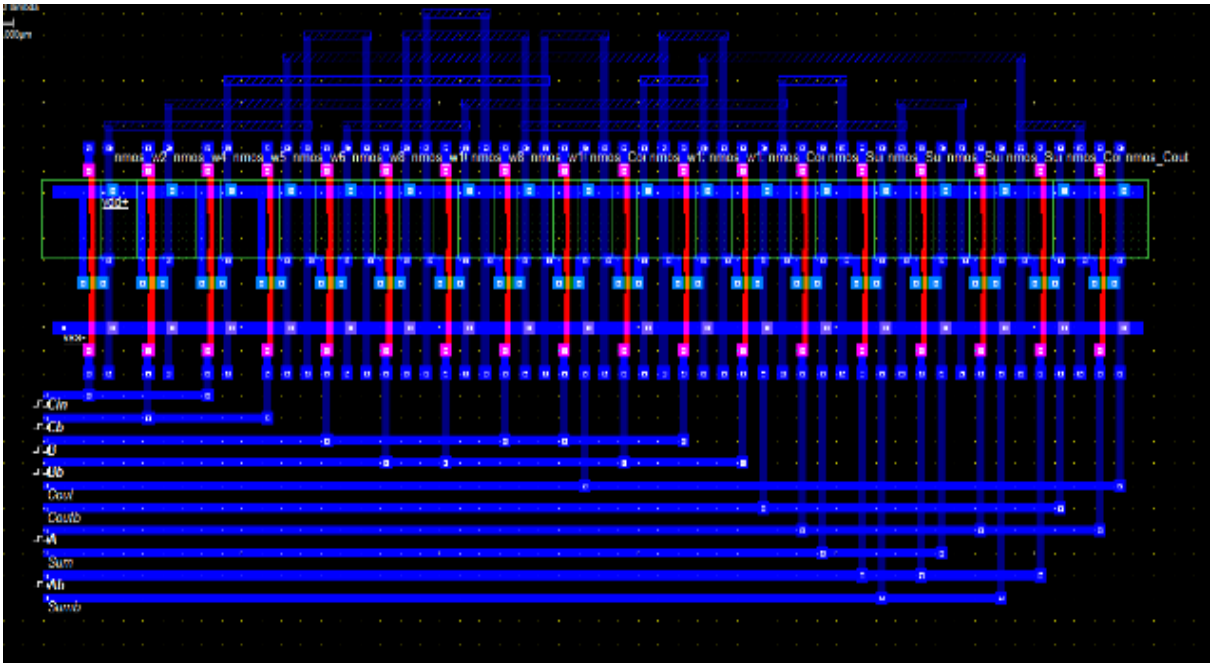


Fig illustrate the simulation output of the proposed ALFA cell. The outputs are represented as a sum, carryout. The layout design is carried out using the 90nmprocesswithapowersupplyvoltage of1.2V. A6metallayer is utilized during the designprocess.

4.0 Conclusion

The ALFA cell has lower power consumption than that of the other versions of the full adder cell because of energy recycling. An ultra-power optimized ALFA cell is proposed using adiabatic logic with the aid of lower occupational area. The performance analysis of full adders in different logic styles is carried out with the focus on obtaining optimized power consumption

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